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PATENT-FAMILY:

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PAGES	MAIN-IPC	
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APPLICATION-DATA:

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INT-CL (IPC): H01L023/02

ABSTRACTED-PUB-NO: US20020074147A

BASIC-ABSTRACT: NOVELTY - Bump chip copper lead frame (100) and package,

comprises a semiconductor die coupled to bump terminals (110), formed by

stamping a plurality of leads (108) with formed stress tabs. The leads are

coplanar with the die carrier (106). The package is encapsulated using one

sided process. The bumps terminals and the die are connected by a wire, where

the die has connection areas for direct connection to the bump terminals.

DETAILED DESCRIPTION - The device inclu

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conductive ground plane 23. Therefore, any overvoltage spikes which enter the package through any input/output lead or conductive pad can immediately pass through the variable voltage protection component 1 to the conductive ground plane 23. The variable voltage protection component 1 can be connected to conductive leads 33 by conductive adhesive or other appropriate means. In addition, the variable voltage protection component can be stamped and heat laminated directly to the leads in a manner similar to tape automated bonding.

[0071] FIG. 15 shows a device 97 utilizing the variable voltage protection component 1 to contact a predetermined pattern of signal leads 99 and ground leads 101. A conductive strip 103 has a pattern of conductive bumps 105, which are etched, stamped or machined to match a predetermined pattern of ground leads 101. The variable voltage protection component 1 is placed between the conductive bumps 105 is flattened off to be even with the conductive bumps 105. A layer 107 of conductive material, such as conductive epoxy or conductive adhesive, is applied to the conductive bumps 105 and variable voltage protection component 1 to match the predetermined pattern of signal leads 99 and ground leads 101. When one of the signal leads 99 experiences an overvoltage spike, the variable voltage pr